F21 Microprocessor

Preliminary specifications 9/98

F21 contains a CPU, a memory interface processor, two analog I/O coprocessors, an active message serial network coprocessor, and a parallel I/O port on a small custom VLSI CMOS chip.

CPU 0 operand stack machine design
27 instructions (2ns + memory access)
20 bit data bus, 21 bit address bus
four 5 bit instructions / 20 bit word

Memory Interface
20 bit DRAM 256K words or 1M words
35-60ns onpage, 112-200-ns offpage
20 bit SRAM 16K words
20ns to 40ns
8 bit SRAM/ROM 1M byte
150ns to 250ns access

Software adjustable -40%,-20%, +20%

Analog I/O coprocessor (externally clocked)
40 Mhz maximum sample rate
6 -8 bit resolution
DMA w/ input and/or output
CPU interrupt instruction at end of buf

Video I/O coprocessor (externally clocked)
Composite video input for genlock*****
Composite video output*****
RGB video output
16 colors w/ transparent color w/ genlock*****
programmable display formats
CPU interrupt and branch instructions

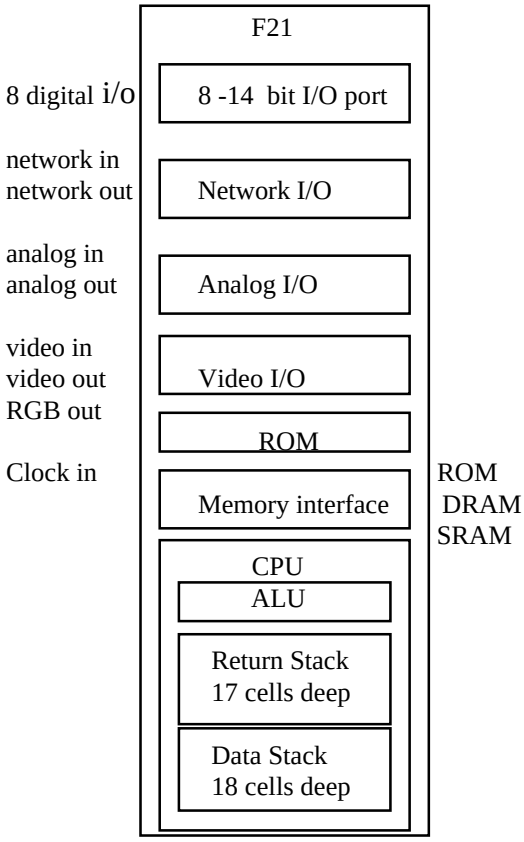
Network I/O coprocessor (externally clocked)
Active Messages (DMA and interrupt)
Indiviual and group addresses
DMA to or from network
CPU interrupts from active message
LAN or SMP

8 - 14 bit bidirectional parallel port

Real Time Clock

32 Words ROM*

***** not on F21d Prototype



CPU instruction time 2ns
Memory setup time 8ns
Minimum memory access 18ns
Maximum sustained mips SRAM 222
(4 instructions per 18ns) (DRAM 111)

External parts required for system:
5x 256K/1Mx4 DRAM or 2x 1Mx16 and/or
3x 8/32Kx8 10 to 35ns SRAM and/or
1x 8K-1Mx8 boot ROM/EPROM/NVSRAM

3V or **5**V, **50mw** (est.) low power operation
68 Pin PLCC in production, CLCC on F21d

Ultra Technology (510) 848-2149
2512 10th St. Berkeley, CA 94710
support@UltraTechnology.com
www.UltraTechnology.com

F21 Microprocessor

Preliminary specifications 9/98

Central Processing Unit

Register	Name	Use
PC	Program Counter	incremented by last instruction in a word, or set by jump, call, return
A	Address Register	Memory access with @A, @A+, !A, !A+, set with A!, read with A
T	Top of Data Stack	all ALU operations use T as the implied operand
S	Second item on data stack used in some ALU operations	
S2 // **S11**	data stack	16 deep circular stack below Tand N
R	Top of Return Stack	Memory access w/ @R+ !R+, used in CALL, return, push and pop
R1 // **R10**	return stack	16 deep circular stack below R, used in call - return, or for temp data

Code	Name	Description	**Forth** (with a variable named A)
00	else	unconditional jump	ELSE
01	T0	jump if T0-19 is false w/ no drop	DUP IF
02	call	push PC+1 to R, jump	:
03	C0	jump if T20 is false	CARRY? IF
06	RET	pop PC from R (subroutine return)	;
08	@R+	fetch from address in R, increment R	R@ @ R> 1+ >R
09	@A+	fetch from address in A, increment A	A @ @ 1 A +!
0A	#	fetch from PC+1, increment PC	LIT
0B	@A	fetch from address in A	A @ @
0C	!R+	store to address in R, increment R	R@ ! R> 1+ >R
0D	!A+	store to address in A, increment A	A @ ! 1 A +!
0F	!A	store to address in A	A @ !
10	com	complement T	-1 XOR
11	2*	left shift T, 0 to T0	2*
12	2/	right shift T, T20 to T19	2/
13	+*	add S to T if T0 is true	DUP 1 AND IF OVER + THEN
14	-or	exclusive-or S to T	XOR
15	and	and S to T	AND
17	+	add S to T	+
18	pop	pop R, push to T	R>
19	A	push A to T	A @
1A	dup	push T to T	DUP
1B	over	push S to T	OVER
1C	push	pop T, push to R	>R
1D	A!	pop T to A	A !
1E	nop	delay 2ns	NOP
1F	drop	pop T	DROP

F21 Microprocessor
Preliminary specifications 9/98
Central Processing Unit

Instruction Timing

All F21 instructions execute in 2ns. Memory access for instruction fetch and data fetch and store must be added in to calculate timing. F21 performs an instruction prefetch as soon as the last memory access instruction has executed. In a sequential stream of stack based operations the limiting factor will be memory setup and access times. With 12ns SRAM will F21 will add a 8ns memory setup time to provide prefetch of an instruction word every 20ns from SRAM. At 4 instructions per 20ns this is 200 MIPS maximum sustained rate.

DUP DUP DUP DUP would begin the next instruction prefetch at the same time as the first DUP.

A! @A+ DUP DUP would not begin the next instruction prefetch until after the execution of the @A+ memory access instruction. The timing would be 2ns for A!, 2ns for @A+, 8ns for the memory setup for the data access, 12ns - 250ns for data read from memory, 2ns for DUP, 2ns for DUP, then the remainder of the time to complete the prefetch of the next instruction word which began at the same time as the first DUP.

Interrupts

The CPU can be interrupted by each of the three I/O coprocessors. The timing of these interrupts depends on the external I/O clock signal and the sequence of instructions executed by the I/O coprocessor.

The coprocessors normally perform I/O directly to or from memory as they execute their own instruction sequences from memory. When they encounter an interrupt instruction they use the CPU to refill or empty I/O buffers, and perform pre- or post-processing of network data.

Ultra Technology
2512 10th St.
Berkeley, CA 94710

(510) 848-2149
support@UltraTechnology.com
www.UltraTechnology.com

F21 Microprocessor
Preliminary specifications 9/98
Analog and Video I/O Coprocessors

Analog I/O Coprocessor

The Analog I/O Coprocessor has a control register where the CPU can set or read the bits. This processor can read and/or write to memory as it times its samples by counting down from a timing register and the external I/O clock signal. It can read a cell from memory, send 8 bits of data to the analog D/A and read the analog A/D and write 8 bits back to the cell in memory at data rates of up to 40 MHz.

The Analog I/O Coprocessor can interrupt the CPU to pre or post process analog data and to fill or empty data buffers. The CPU can also set the analog clock and Analog I/O Coprocessor control register to start and stop the Analog Coprocessor.

This processor may often be used for audio signals, but is fast enough to digitize and generate video and other high speed analog signals.

It is a programmable self timed D/A, A/D pair with DMA and CPU interrupt capabilities.

Video I/O Coprocessor

The Video I/O Coprocessor has a control register where the CPU can set or read the bits. This processor can read and/or write to memory as it times its samples by counting down from a timing register and the external I/O clock signal. It can read video data from memory and generate NTSC or RGB video in different resolutions. F21 provides 15 colors and a transparent color with genlock when used with an external video source. (*)

The Video I/O Coprocessor can interrupt the CPU to pre or post process video data and to fill or empty data buffers. The CPU can also set the video clock and Video I/O Coprocessor control register to start and stop the Video Coprocessor.

* No composite video I/O on F21c prototype

Ultra Technology
2512 10th St.
Berkeley, CA 94710

(510) 848-2149
support@UltraTechnology.com
www.UltraTechnology.com

F21 Microprocessor
Preliminary specifications 9/98
Serial Network I/O Coprocessor

Active Message Serial Network I/O Coprocessor

The Network I/O Coprocessor has a control register where the CPU can set or read the bits. This processor can read and/or write to memory as it times its samples by counting down from a timing register and the external I/O clock signal. It can recognize its address in a serial packet and perform a DMA to memory with a data transfer and interrupt the CPU. The CPU may then initiate the sending of serial data out of the unit via a DMA transfer.
When interrupted the CPU can pre- or post-process network data. It is a simple form of an active message with an address, data, and a DMA transfer and CPU interrupt if the address in a message matches the one in the network address control register.

Network Topology

With one input and one output pin an F21 has all the hardware needed to connect chips together to form a ring. The network output pin may be tri-stated to provide fan out and fan in to provide other topologies. Software must arbitrate the network to avoid collision.

Bandwidth Limitations

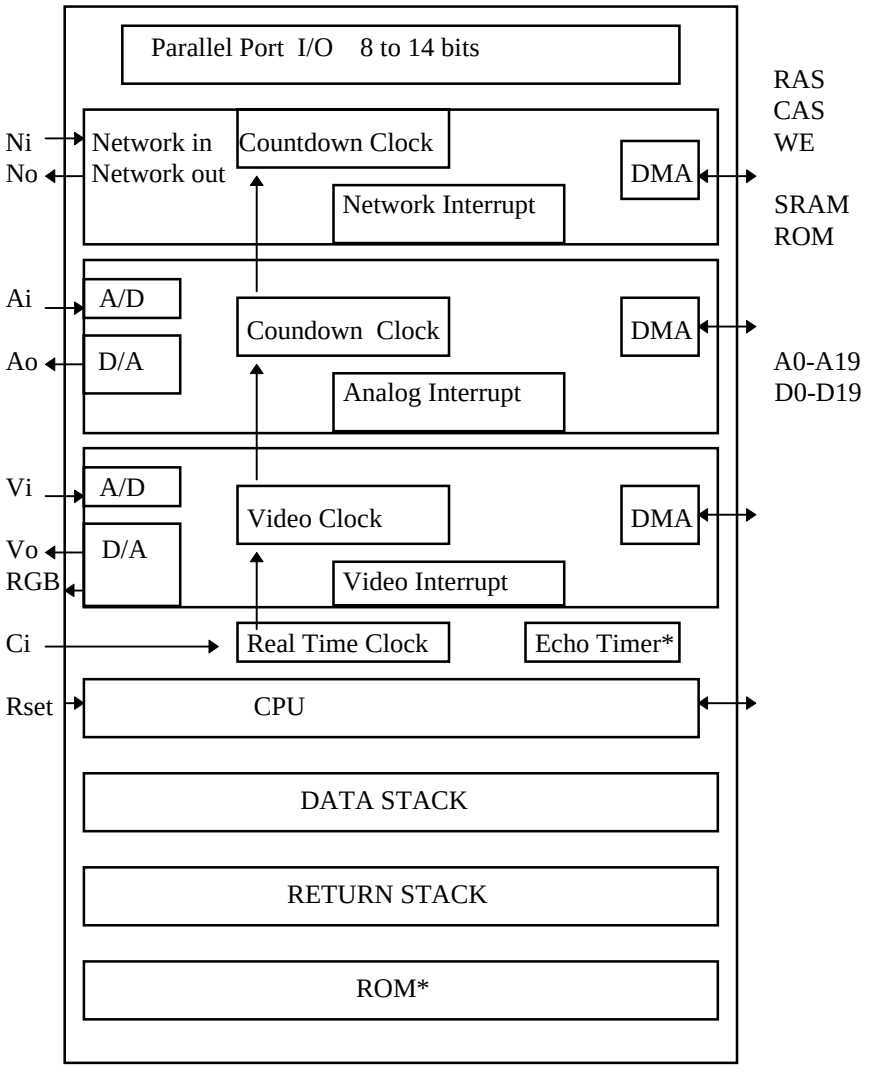
An F21will be memory bandwidth limited. The CPU can execute instructions at 500 MIPS internally, but external memory access limits speed to 333 in ROM, 222 in SRAM or 111 MIPS in DRAM. This is the maximum speed for sequential stack operations if the CPU is the only processor accessing memory. The Analog, Video, and Network coprocessors are timed from and external source and will each get memory access before the CPU. The CPU will only get as much memory access as is left over after the coprocessors are done. Each of the coprocessors is capable of using the entire memory bandwidth if programmed to do so. It is thus not possible to get the maximum specified performance from each of the processors at the same. time. Each node in a F21 SMP system can however be used as a general purpose computing node or as a dedicated I/O processor. This provides up to 2 analog inputs, 4 analog outputs, and 8 -12 digital I/O lines on each node of an F21 SMP.

Ultra Technology
2512 10th St.
Berkeley, CA 94710

(510) 848-2149
support@UltraTechnology.com
www.UltraTechnology.com

F21 Microprocessor Diagram

Preliminary specifications 9/98



* no internal ROM or Echo Timer on F21d

Ultra Technology
2512 10th St.
Berkeley, CA 94710

(510) 848-2149
support@UltraTechnology.com
www.UltraTechnology.com

F21 Microprocessor

Preliminary specifications 9/98

```
F21d clcc
                  Pin 1
                   |
     PA 9 8 7 6 + - 5 4 3 2 1 P0 RA RO RS
    R                                  CS
   Ni                                  P+
   No                                  P-
   PB                                   W
   Ao                                   9
   Ai                                   8
    C                                   7
    B                                   6
   A+              F21d                 5
    R              pins                 4
    G                                   3
   A-                                   2
   19                                   1
   18                                  A0
   17                                  D0
   16                                   1
   15                                   2
   14                                   3
     13 12 11 10 + + - - 9 8 7 6 + - 5 4
```

F21 Wiring Diagram for system with 3 sockets, 68 pin CLCC F21d in a hole through socket, PROM, and DRAM SIMM sockets.

```
512K ROM
+      +*            BOTTOM VIEW
12    10
11    DF                    *
DE    DC      RS RA P1 P3 P5  + P7 P9 RE
DD    A7   CS RO P0 P2 P4  - P6 P8 PA So Si
A8    A6    -  +                     Ao PB
A9    A5   A9  W                     C  Ai
DB    A4   A7 A8                     +  B
-     A3   A5 A6        F21d         G  R
DA    A2   A3 A4                     13 -
RO    A1   A1 A2                     11 12
D7    A0   D0 A0                     DF 10
D6    D0   D2 D1 D4  - D6 D8  -  + DA DC DE
D5    D1      D3 D5  + D7 D9  -  + DB DD
D4    D2
D3     -
*
D0 D1 D2 D3 +  A0 A2 A4 A6 D5 D6 D7 A7  + A9 RS . wrap
 - 10 11 12 13  . A1 A3 A5  .  .  .  .  . A8 .  .
                     wrap . CS  + RS  .  .  .  .  .  .  .  .  .  .  .  .  -
          SIM             .  - CS CS  . WE D8 D9 DA DB DC  + DD DE DF  .  .  .

* Pin 1
10-13 are D10-D13
Connect all + and all -.  10uF between + and -
Connect labeled pins from F21:
   A0-9, D0-7, DA-12 and RO to ROM
   A0-9, D0-13, CS, RS and W to SIM
On RE, 1uF to -, 100K ohm to +
```


Ultra Technology
2512 10th St.
Berkeley, CA 94710

(510) 848-2149
support@UltraTechnology.com
www.UltraTechnology.com